REMARKS

Reconsideration of this application as amended is requested. By this amendment Applicants have amended claims 1, 4, 19 and 27. Claims 1-27 remain in the case.

The Examiner objected to the drawing figures because words and labels are unreadable, and because Fig. 1 should be labeled "Prior Art." Applicants hereby submit Replacements Sheets for the drawing figures that clearly label Fig. 1 as "Prior Art", and that render the words and labels in general readable. Therefore the Examiner's objection to the drawing is now deemed to be moot.

The Examiner objected to claim 4 because of an informality – "the reference signal frequency" should be changed to –the first frequency– as recited in lines 2-3 of Claim 1. Since claim 4 is an independent claim and not dependent from claim 1, Applicants do not see the need to amend claim 4 since it should be considered solely on its own without reference to any other claims. However Applicants note that lines 2-3 of claim ***4*** do recite "a reference signal having a first frequency", so line 8 has been amended to read "approximating the *first* frequency", rendering the Examiner's objection moot.

The Examiner rejected claims 4-27 under 35 U.S.C. 112, second paragraph, as being indefinite, specifically referring to claims 4, 19 and 27. Claims 5-18 and 20-26 are rejected because of their dependencies on base claims 4 and 19.

Claim 4: With respect to claim 4 the Examiner states that the limitation "a feedback circuit comprising at least said first accumulator and said second accumulator for feeding back an accumulated error to the first accumulator for providing a next value in said sequence of divide ratios" is indefinite as being misdescriptive, referring to Fig. 3 where the feedback circuit feeds back an accumulated error to the first accumulator – the first and second accumulators do not make up the feedback circuit. Applicants have amended claim 4 to recite "a feedback circuit having at least the error output from said

first accumulator and an accumulated error output from said second accumulator as inputs for feeding back" to clearly indicate that the inputs to the feedback circuit are from the two accumulators, not that the accumulators are part of the feedback circuit. Thus claim 4 as amended is deemed to be definite as particularly pointing out and distinctly claiming what Applicants regard as the invention.

Claim 19: Applicants have amended claim 19 in a similar manner to the amendment to claim 4. Thus claim 19 as amended also is deemed to be allowable.

Claim 27: The Examiner states that claim 27 is indefinite for claiming both an apparatus and method of using the apparatus in a single claim, citing *Ex parte Lyell*, 17 USPQ2d 1548. Applicants have amended claim 27 to recite the steps that occur in the modulator to produce the divide ratio sequence so that now claim 27 is a pure method claim. Thus claim 27 as amended is deemed to be definite as particularly pointing out and distinctly claiming what Applicants regard as the invention.

The Examiner also rejected claim 27 under 35 U.S.C. 101 as being directed to neither an apparatus nor a method. However claim 27 as amended is directed to a "method", and is deemed to encompass statutory subject matter.

The Examiner rejected claims 1-10, 12-14 and 19-22 under 35 U.S.C. 102(e) as being anticipated by Lee, while indicating that claims 11, 15-18 and 23-26 contained allowable subject matter. With regards to claims 1 and 4 the Examiner states that Lee in Figs. 1-2 discloses a phase-locked loop-type frequency synthesizer having a reference signal source for providing a reference signal (fref), a programmable oscillator for providing an oscillating signal (fvco), a programmable scaler (102-108) for dividing the oscillating signal from the programmable oscillator according to a sequence of divide ratios to produce a divided signal having a frequency approximating the reference signal frequency, a phase comparator (112) and a modulator (118) for providing the sequence of divide ratios wherein a next value in the

sequence of divide ratios is provided by accumulating an error between a present value in the sequence of divide ratios and an average value of the sequence of divide ratios such that the muliply-accumulated error values are maintained within finite bounds, wherein the modulator has a first accumulator (202) for accumulating an error between a present value in the sequence of divide ratios and an average value of the sequence of divide ratios, a second accumulator (204) for accumulating an error output of the first accumulator, and a feedback circuit (212, 218, 220). Applicants respectfully traverse this improper and nonobvious conclusion by the Examiner.

In contradistinction to Applicants' claimed invention Lee discloses a single-bit sigma-delta modulated fractional-N frequency synthesizer in a phase-locked loop-type circuit having a VCO (like 710 = 230) frequency (fvco = f*N) input to a prescaler (102 = 275), as opposed to a multi-bit sigma-delta modulator as taught by Applicants. The output (fvco/P = f*N/X) of the prescaler is further divided by two values B/A (104, 106), one of which (fvco/(p*B)) is input to a phase detector (112 = 210), to a modulus control (108) and as a clock to a digital sigma-delta modulator (118 = 280). The other input to the phase detector is the reference signal (fref = f*M) divided by R (fref/R), and the output of the phase detector is input to a lowpass loop filter (like 706 = 220) to control the VCO. The other divided prescaler output (fvco/(p*A)) is input to the modulus control, which in turn determines whether the divider of the prescaler is P or P+1. The dual-modulator divider circuit (B/A) is controlled by a bit converter (116) output that converts 0 or 1 from the modulator into 1 and -1. There are two distinctions between Applicants' claimed invention and Lee: 1) Lee takes feedback from the last accumulator and applies it to all the accumulators, while Applicants take feedback from at least the first two accumulators and apply it to the first accumulator; and 2) Lee discloses a single-bit modulator that results in ratios having to be approximately ½ (k/b1 restricted to -0.5 - 0.5 for stable operation, or otherwise stated the overflow detector operates when k/b1 greatly exceeds 0.5), while Applicants disclose a multi-bit modulator that allows a range of ratios not

limited to around ½ (for large values of the ratio the sequence X is represented with many bits (>4), while for smaller values may be represented with only a few bits (<=4)).

Claim 1 as amended recites that the oscillating signal is divided "according to a sequence of at least three distinct divide ratios", i.e., a multi-bit modulator. This is not taught or suggested by Lee. Thus claim 1 is deemed to be allowable as being neither anticipated nor rendered obvious to one of ordinary skill in the art by Lee.

Claim 4 recites that the feedback circuit receives inputs from each of the outputs of the two accumulators for feeding back an accumulated error to the first accumulator. This configuration is neither taught nor suggested by Lee. Thus claim 4 are deemed to be allowable as being neither anticipated nor rendered obvious to one of ordinary skill in the art by Lee.

Since claims 1 and 4 are deemed to be allowable, claims 2, 3 and 5-18 dependent therefrom also are deemed to be allowable.

For the reasons discussed above with respect to the relationship of the accumulators to the feedback circuit as recited in claim 4, claim 19 and claims 20-26 dependent therefrom also are deemed to be allowable as being neither anticipated nor rendered obvious to one of ordinary skill in the art over Lee.

In view of the foregoing discussion and remarks allowance of claims 1-27 as amended is urged, and such action and the issuance of this case are requested.

Respectfully submitted,

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